

**CS 473**  
**Final Exam**  
**December 10, 2004**

The following exam is open book and open notes. You may feel free to use whatever additional reference material you wish, but **no electronic aids** are allowed. Please note the following instructions. There will be a ten point deduction for failure to comply with them:

- start each problem on a new sheet of paper
- write your social security number, but not your name, on each sheet of paper you turn in
- show your work whenever appropriate. There can be no partial credit unless I see how answers were arrived
- be succinct. You may lose points for facts that, while true, are not relevant to the question at hand

You have until 3:00 to finish the exam.

1. (20 points) Floating point arithmetic:

- (a) Add the following pair of IEEE floating point numbers:  $0x40480000 + 0xc0d80000$
- (b) Convert your result into human-readable decimal.

2. (40 points) Superscalar Pipelining

Consider the following sequence of MIPS instructions:

```
add  $1, $2, $3
lw   $7, 200($1)
sw   $6, 100($7)
sw   $1, 100($4)
sw   $7, 300($10)
add  $8, $9, $10
sub  $11, $8, $1
add  $5, $1, $3
```

- (a) Draw arrows showing all of the dependencies between the registers in instructions in this code. Note that if a register is set by an instruction, and then read by two different instructions, there are two dependencies.
- (b) Draw a Gantt chart showing how this code is executed in the superscalar pipeline from HW 5.
- (c) Reorder the code to execute as quickly as possible and draw another Gantt chart showing how the modified code is executed.

3. (15 points) Cache

- (a) A computer with a 32-bit address has a 64K, 16-way set-associative cache with a 16 byte block size. What are the tag, index, and byte offset for address  $0x12345678$ ?
- (b) A computer has a 13 bit index and 5 bit byte offset. If it uses a 32 bit address, what is the width of the tag field? If it has a 512K cache, how set-associative is it?

4. (20 points) Virtual Memory

Following are the PDBR and some memory addresses from an Intel. What is the result of each of the following memory accesses (all the numbers are hexadecimal)?

- (a) Kernel mode write to 097e8b68
- (b) user mode read from 17e289f0
- (c) User mode write to 5957d91c

PDBR: 3adcc000

| Address  | Contents |
|----------|----------|
| 19af391c | 47c476d9 |
| 2e673fa0 | 44aed006 |
| 2fa4d9f0 | 4e01295f |
| 3adcc094 | 2e673006 |
| 3adcc17c | 4f244003 |
| 3adcc594 | 70b29007 |
| 44aedb68 | 1270734d |
| 4f2448a0 | 2fa4d003 |
| 70b295f4 | 19af3007 |

5. (5 points) Input/Output

Suppose a computer has an IO subsystem that has a not-PCI but very convenient 100 MHz, capable of performing a 4-byte transfer on every bus cycle. Address and data are multiplexed (so every transfer requires one address cycle followed immediately by several data cycles).

- (a) What is the theoretical maximum amount of data that can be transferred per second (the throughput), given an unlimited number of data cycles in a burst?
- (b) What is the actual amount of data transferred per second if each transfer has exactly one four-byte data cycle?